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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/509,863	06/10/2005	Guido Plangger	CH02 0005 US	5331

65913 7590 06/20/2008

NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
NGUYEN, VINH P	

ART UNIT	PAPER NUMBER
2829	

NOTIFICATION DATE	DELIVERY MODE
06/20/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/509,863	PLANGGER ET AL.	
	Examiner	Art Unit	
	VINH P. NGUYEN	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-12 and 14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-12 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the features of "a detection circuit","an activation circuit" and "test line" as recited in claim 1, the features of "means for detecting the switching state of said switching element" as recited in claim 10 and means for applying a first voltage to said first test point" ,"means for applying a second different voltage to said second test point" and "means for detecting a current flow between said first and second test points" as recited in claim 11 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. Claims 1-6,9-12 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, it is unclear what "an activation circuit", "test line" and "a detection circuit for detecting the switching state of said switching circuit" comprise of . Are they shown in any of drawings?

In claims 8 and 14, "said group of test transistors" and "said test point" have no antecedent basis.

In claim 10, it is unclear what "means for detecting the switching state of said switching element" comprises of. Is it shown in any of drawings?

In claim 11, it is unclear what "means for applying a first voltage to said first test point" ,"means for applying a second different voltage to said second test point" and "means for detecting a current flow between said first and second test points" comprise of. Are they shown in any of drawings?

The dependent claims not specifically address share the same indefiniteness as they depend from rejected base claims.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-6 and 10-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Andersen et al (Pat # 6,211,693).

As to claim 1, Andresen et al disclose a testing apparatus as shown in figures 1-2. According to Andresen et al, a cascade circuit includes an electronic component (Q1,Q4) to be protected by high voltage and a cascade element (Q2,Q3) having the steps of arranging a test node (A,C) between said electronic element (Q1) and said cascode element (Q2), allocating a switching element (Q6,Q7) to said test node (A,C) and connecting said switching element to said test node, said switching element having a plurality of switching states and being constituted such that its switching state is changed when the voltage at said test node exceeds or falls below a given voltage limit, activating said cascode element (Q2,Q3) by a biasing network (21) and detecting the switching state of said switching element by a test circuit (10) and wherein said cascode circuit comprises a plurality of electronic elements (Q1,Q4) to be protected from high voltage and a plurality of cascode elements (Q2,Q3), each cascode element being connected to an electronic element, and wherein a group of switching elements (Q6,Q7) is connected by at least one test line (electrical conductor/teminal at the end of each of the switch element (Q6,Q7) connected to contact points (A) and (C)) so that the electric signal on said at least one test line indicates whether the switching state of at least one switching element from said group of switching elements is in a changed switching state (see column 4, lines 10-48).

As to claims 2 and 6, the voltage limit at the test node (A,C) is chosen to be an upper voltage limit Vcchv (5V) applicable to the electronic element (Q1,Q4) if the electronic element (Q1,Q4) is connected to a ground-voltage line (ground line at the end of the electronic element (Q4)) when the cascade (Q2,Q3) are defected, then there is a current flowing in the test circuit (10).

As to claim 3, wherein the switching element (Q6,Q7) is a test transistor , the gate of the test transistor (Q6,Q7) is connected to the test node (A,C), the source of the test transistor (Q6,Q7) is connected to a first test point (D) and a drain of the test transistor (Q6,Q7) is connected to a second different voltage) and a current flow between the first test point (D) and the second test points (E) is detected by the test circuit (10).

As to claim 4, the detection of a current flow used for testing a correct or an incorrect working of the cascade circuit (Q2,Q3) or for determining a voltage on the test node (A,C) (see column 4, lines 9-48).

As to claim 6, the electronic element (Q4) and the test transistor (Q6) of Andresen et al are N-MOS field effective transistors of a first channel conduction type

As to claim 10, Andresen et al disclose a testing apparatus as shown in figures 1-2 having an electronic element (Q1,Q4) to be protected from high voltage, a cascade element (Q2 ,Q3) connected to the electronic element (Q1,Q4), a test node (A ,C),a test circuit (10) including a plurality of switching elements (Q6,Q7) with a plurality of switching state and being constitute

such that its switching state is changed when the voltage at the test node (A,C) exceeds or fails below a given voltage (see column 4, lines 9-48). It appears that the test circuit (10) of Andresen et al inherently includes means for detecting the switching sate of the switching elements in order to determine whether there is a current or no current flowing through the switching elements (Q6, Q7) (see column 4, lines 9-48).

As to claim 11, the switching element (Q6,Q7) is a test transistor , the gate of the test transistor (Q6,Q7) is connected to the test node (A,C), the source of the test transistor (Q6,Q7) is connected to a first test point (D) and a drain of the test transistor (Q6,Q7) is connected to a second different voltage). It appears that the device of Andresen et al inherently includes means for applying the first and second voltage to the first and second test points in order to provide voltage signals at those test points . Furthermore, the device of Andresen et al also inherently includes means for detecting a current flow between the first test point (D) and the second test points (E) in the test circuit (10) in order to determine the defected cascode element (Q2,Q3).

As to claim 12, the electronic element (Q4) and the test transistor (Q6) of Andresen et al are N-MOS field effective transistors of a first channel conduction type.

5. Applicant's arguments with respect to claims 1-6,8-12 and 14 have been considered but are moot in view of the new ground(s) of rejection.

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Dinteman et al (Pat # 5,942,922) disclose inhibitabble,continuously terminated differential drive circuit for an integrated circuit tester.

Kirkpatrick et al (Pat # 4,656,417) disclose test circuit for differential cascode voltage switch.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VINH P. NGUYEN whose telephone number is 571-272-1964. The examiner can normally be reached on 6:30AM-4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, HA T. NGUYEN can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/VINH P NGUYEN/
Primary Examiner
Art Unit 2829